

## CLAIMS

What is claimed is:

1. A capacitor comprising:
  - a plurality of first conductive layers;
  - a plurality of second conductive layers interleaved with the first conductive layers;
  - a plurality of dielectric layers separating adjacent conductive layers;
  - a plurality of first conductive vias to electrically connect the first conductive layers;
  - a plurality of second conductive vias to electrically connect the second conductive layers; and
  - wherein openings are formed in the capacitor to enable pins from an integrated circuit package to pass through.
2. The capacitor of claim 1, wherein the openings has a diameter which is greater than a diameter of each pin from the integrated circuit package such that a defined distance is maintained between an edge of each respective opening and each respective pin.
3. The capacitor of claim 1, wherein the openings are arranged to coincide with at least four pins from the integrated circuit package that are located directly underneath a semiconductor die.
4. The capacitor of claim 1, further comprising:
  - a plurality of first conductive terminals coupled to the plurality of first conductive vias; and
  - a plurality of second conductive terminals coupled to the plurality of second conductive vias.
5. The capacitor of claim 4, wherein

the first conductive terminals are configured for coupling to a ground plane provided in an IC package; and

the second conductive terminals are configured for coupling to a power plane provided in the IC package.

6. A system comprising:

an integrated circuit (IC) coupled to a first side of an IC package; and

a capacitor attached to a second side of the IC package underneath the integrated circuit, the capacitor having openings to enable pins from the IC package to pass through.

7. The system of claim 6, wherein the openings are arranged to coincide with at least four pins from the IC package that are located directly underneath the integrated circuit.

8. The system of claim 6, wherein the capacitor comprises:

a plurality of first conductive layers coupled to a first node in the integrated circuit;

a plurality of second conductive layers interleaved with the first conductive layers, the second conductive layers coupled to a second node in the integrated circuit; and

a plurality of dielectric layers separating adjacent conductive layers.

9. The system of claim 8, wherein the capacitor further comprises:

a plurality of first conductive vias to electrically connect the first conductive layers;

a plurality of second conductive vias to electrically connect the second conductive layers;

a plurality of first conductive terminals coupled to the plurality of first conductive vias; and

a plurality of second conductive terminals coupled to the plurality of second conductive vias.

10. The system of claim 6, wherein the openings formed in the capacitor has a diameter which is greater than a diameter of each pin from the integrated circuit package such that a defined distance is maintained between an edge of each respective opening and each respective pin.

11. The system of claim 6, further comprising:  
a socket to receive the pins from the IC package

12. The system of claim 11, wherein the socket is a full-grid socket that is capable of receiving power and ground pins located on a backside of the package under a die shadow.

13. The system of claim 11, wherein the socket is shaped to accommodate the capacitor attached to the IC package.

14. The system of claim 6, wherein the integrated circuit is embodied in a form of a semiconductor die.

15. A method comprising:  
providing a capacitor with a plurality of openings;  
providing an integrated circuit (IC) housed by an IC package;  
passing pins from the IC package through the openings formed in the array capacitor;  
positioning the capacitor on a backside of the IC package directly underneath the integrated circuit;  
electrically connecting the capacitor to the IC package.

16. The method of claim 15, further comprising:  
electrically connecting the IC package to a socket.

17. The method of claim 15, wherein the capacitor comprises:

a plurality of first conductive layers;  
a plurality of second conductive layers interleaved with the first conductive layers; and  
a plurality of dielectric layers separating adjacent conductive layers.

18. The method of claim 17, wherein electrically connecting the capacitor to the IC package comprises:

electrically coupling the first conductive layers to a first node in the integrated circuit; and

electrically coupling the second conductive layers to a second node in the integrated circuit.